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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,577	02/23/2004	Donald Thomas McGrath	RD-27645-2	9571

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GENERAL ELECTRIC COMPANY
GLOBAL RESEARCH
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NISKAYUNA, NY 12309

EXAMINER	
SAYADIAN, HRAYR	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,577	MCGRATH, DONALD THOMAS	
	Examiner	Art Unit	
	Hrayr A. Sayadian	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-29* is/are pending in the application.

4a) Of the above claim(s) *27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26,28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED OFFICE ACTION

Notice Re Change of Examiner and A.U. Number

1. Applicant should notice the change in Examiner, and A.U. number from 2828 to 2815. Applicant should use 2815 as the A.U. number in further correspondence regarding this Application.

2. Claim 27 has been withdrawn from consideration because it is directed toward the combination of a BFL and a chopping circuit that was the subject of the previous parent application serial number 09/682,863. Note the restriction requirement in 09/682,863. The search for the combination of the BFL and the chopping circuit now present was not required for the BFL circuit. This places an additional burden on the examiner. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 27 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and M.P.E.P. 821.03.

Objection to the March 14, 2007 Amendment– New Matter

2. The amendment filed on 3/14/2007 is objected to under 35 U.S.C. § 132(a) because it introduces new matter into the disclosure of the invention by way of amending claims 26 and 28.

The amendments to the claims lack support in the originally filed disclosure of the invention. Specifically, the originally filed disclosure of the invention does not disclose first and second electrical nodes comprising "redistribution point(s) configured to recognize and transmit ... BFL level-shifting/inverter circuit," as now recited in the claims. This is of special concern considering the early filing date of this application.

35 U.S.C. § 132(a) prohibits any "amendment [from] introduce[ing] new matter into the disclosure of the invention." Accordingly, Applicant is required to cancel, in the reply to this Office Action, the new matter introduced by the amendment to the specification.

Objections to the Drawings

3. The drawings are objected to under 37 CFR § 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the now recited in claims 26-29 (and objected to as new matter; see, above New Matter objection to amending the claims by now reciting the first and second nodes comprising "redistribution point(s) configured to recognize and transmit ... BFL level-shifting/inverter circuit,") must be shown or these features canceled from claims 26-29.

Corrected drawing sheets complying with 37 CFR § 1.121(d) are required in reply to the Office Action to avoid abandonment of the application. 35 U.S.C. § 132(a) prohibits any "amendment [from] introduce[ing] new matter into the disclosure of the invention." Accordingly, new matter should not be introduced by either addition or deletion.

Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement-sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement-sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR § 1.121(d).

The next Office Action will notify Applicant of the required correction if the changes are not acceptable.

The objection to the drawings will not be held in abeyance.

Objection to the Specification

4. The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact

> terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. The specification is objected to as failing to provide proper antecedent basis for the subject matter in claims 26-29. See 37 CFR § 1.75(d)(1) and M.P.E.P. § 608.01(o). Correction of the following is required:

The detailed description must be amended to provide antecedent basis for first and second electrical nodes comprising "redistribution point(s) configured to recognize and transmit ... BFL level-shifting/inverter circuit," as now recited in the context of the claims.

35 U.S.C. § 132(a) prohibits any "amendment [from] introduce[ing] new matter into the disclosure of the invention." Accordingly, new matter should not be introduced by either addition or deletion.

6. The specification is objected to under 35 U.S.C. § 112, first paragraph, as failing to provide an enabling description for the subject matter in claims 26-29.

One of ordinary skill in the art would not be able to make and use the invention in claims 26-29 without undue experimentation. Specifically, it is unknown how is one to first and second electrical nodes comprising "redistribution point(s) configured to recognize and transmit ... BFL level-shifting/inverter circuit," as now recited in the context of the claims.

Claim Rejections - 35 U.S.C. § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 26, 28, and 29 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. These claims contains subject matter not

described in the specification in such a way as to reasonably convey to one skilled in the relevant art that Applicant, at the time the application was filed, had possession of the claimed invention.

Correction is required. 35 U.S.C. § 132(a) prohibits any "amendment [from] introduce[ing] new matter into the disclosure of the invention." Accordingly, new matter should not be introduced by either addition or deletion.

9. Claims 26, 28, and 29 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. These claims contain subject matter not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. One of ordinary skill in the art would not know how to make or use, or both, first and second nodes comprising "redistribution point(s) configured to recognize and transmit ... BFL level-shifting/inverter circuit."

Correction is required. 35 U.S.C. § 132(a) prohibits any "amendment [from] introduce[ing] new matter into the disclosure of the invention." Accordingly, new matter should not be introduced by either addition or deletion.

10. Claims 26, 28, and 29 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter Applicant regards as the invention.

Specifically, the meaning and scope of the recitations the first and second nodes comprising "redistribution point(s) configured to recognize and transmit ... BFL level-shifting/inverter circuit" is indefinite.

Correction is required. 35 U.S.C. § 132(a) prohibits any "amendment [from] introduce[ing] new matter into the disclosure of the invention." Accordingly, new matter should not be introduced by either addition or deletion.

Claim Rejections - 35 U.S.C. § 103

11. Claims 26, 28, and 29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 4,661,726 to Baird [hereinafter "Baird"].

At least in Figure 4 and the relevant text, Baird discloses a buffered field effect transistor (BFL) level-shifting/inverter circuit having an "inverter stage" input "IN", a first depletion mode inverter, that receives i.e. is responsive to the "inverter stage" input IN signal at a depletion mode MOSFET 30, and a buffered field effect transistor logic stage. The buffered field effect transistor logic stage has a first depletion mode MOSFET 32 and a second depletion mode MOSFET 37. A voltage drop or what is commonly called a level shifter is connected between the first and second transistors and is composed of elements like 33, 34.

The node between element 32 and 33 forms a first output and the node between element 37 and 36 forms a second output. It is important to note that column 1, around line 50 of Baird recites that the logic gates of the invention "will therefore be described in terms of such logic gates" i.e. MESFETs but Baird is also very specific that "[t]hose skilled in the art will readily perceive that the invention (which includes the BFL of Figure 4) may be used with any logic gate utilizing depletion mode FETs. Such FETs may be metal oxide semiconductor field effect transistors (MOSFETs) ... (emphasis added) ..." Thus the Figure 4 embodiment is clearly applicable to MOSFETs and includes depletion mode MOSFETs.

Baird is silent on the type of depletion mode MOSFET, i.e. NMOS or PMOS. However, NMOS and PMOS depletion mode MOSFETs are conventional forms of depletion mode MOSFETs. (And Applicant does not dispute their well known and conventional nature).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used depletion mode NMOS transistors for the transistors of Baird because, as the Baird reference is silent on the exact depletion mode FET used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent depletion mode FET such as the conventional depletion mode MOSFET.

In view of the 112(1,2) objection and rejection of the claims, and absent specifics in the claims of how the first and second nodes structurally comprise "redistribution point(s) configured to recognize and transmit ... BFL level-shifting/inverter circuit," the scope of these recitations is treated broadly and found to read on the various signals in Baird transmitting through the first and second nodes.

The device disclosed by Baird is capable of performing the recited functions and as such Baird meets these functional limitations (See In re Schreiber, 128 F. 3d 1473, 1477, 44 USPQ2d 1429, 1431 fled. Cir. 1997).

12. Claim 28 and 29 are rejected under 35 U.S.C. § 103(a) as being unpatentable Baird, further in view of U.S. Pat. Nos. 4,810,907 and 6,559,068 to Tohyama [hereinafter "Tohyama"] and Alok et al. {hereinafter " "Alok"], respectively.

At least in Figure 4 and the relevant text, Baird discloses a buffered field effect transistor (BFL) level- shifting/inverter circuit having an input "IN", a first depletion mode inverter that receives the IN signal at a depletion mode MOSFET 30, and a buffered field effect transistor logic stage.

The buffered field effect transistor logic stage has a first depletion mode MOSFET 32 and a second depletion mode MOSFET 37. A voltage drop or what is commonly called a level shifter is connected between the first and second transistors and is composed of elements like 33, 34. The node between element 32 and 33 forms a first output and the node between element 37 and 36 forms a second output. It is important to note that column 1, around line 50 of Baird recites that the logic gates of the invention "will therefore be described in terms of such logic gates" i.e. MESFETs, but Baird is also very specific that "[t]hose skilled in the art will readily perceive that the invention (which includes the BFL of Figure 4) may be used with any logic gate utilizing depletion mode FETs. Such FETs may be metal oxide semiconductor field effect transistors (MOSFETs) ... (emphasis added)." Thus the Figure 4 embodiment is clearly applicable to MOSFETs and includes depletion mode MOSFETs. Baird is silent on the type of depletion mode MOSFET, i.e. NMOS or PMOS.

Alok however discloses that silicon carbide NMOS and PMOS depletion mode MOSFETs formed on a silicon carbide substrate are conventional forms of depletion mode MOSFETs (See entire reference.) Alok also motivates using of Silicon Carbide transistors because they are ideal for "high voltage, high frequency and high temperature" (See column 1, around line 33).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used silicon carbide depletion mode NMOS transistors formed on a silicon carbide substrate for the transistors of Baird because, as the Baird reference is silent on the exact depletion mode FET used one of ordinary skill in the art would have been motivated to use any art- recognized equivalent depletion mode FET such as the conventional silicon carbide depletion mode NMOS MOSFET formed on a silicon carbide substrate. Additionally one of ordinary skill would have been motivated to make the combination because of the higher voltage handing, the higher frequency capabilities and the higher temperature handing capabilities as compared to conventional Si based MOS devices as disclosed by Alok. Silicon carbide MOSFETs are better FETs.

Baird is silent on the use of resistor(s) for the voltage drop circuit.

Tohyama however shows that the resistor, the diode and the "diode connected "FET like of Baird are all art-recognized equivalent voltage drop circuits for use in BFTs.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the voltage drop circuit of Baird with a resistor because two voltage drop circuits are well known to be equivalent in the art as taught by Tohyama.

Because the combination made obvious above includes depletion mode NMOS transistors, this circuit, being the same as that claimed, is configured to operate with a negative direct current bias on each of the gates with respect to the associated channel.

In view of the 112(1,2) objection and rejection of the claims, and absent specifics in the claims of how the first and second nodes structurally comprise "redistribution point(s) configured to recognize and transmit ... BFL level-shifting/inverter circuit," the scope of these recitations is treated broadly and found to read on the various signals in Baird transmitting through the first and second nodes.

Response to Applicant's Argument

13. Applicant's argument has been fully considered, but is found not to overcome the prior art rejections.

Applicant argues that the prior art fails to disclose first and second electrical nodes comprising "redistribution point(s) configured to recognize and transmit ... BFL level-shifting/inverter circuit."

Applicant is directed to the explanation above of the objection to and rejection of these recitations.

CONCLUSION

14. A shortened statutory period for reply to this Office Action is set to expire **THREE MONTHS** from the mailing date of this Office Action. Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hrayr A. Sayadian whose telephone number is (571) 272-7779. Examiner Sayadian can normally be reached Monday through Friday, 7:30 am – 4:00 pm.

If attempts to reach Examiner Sayadian by telephone are unsuccessful, his supervisor, SPE Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HAS

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800